

Appl. No. 10/707,221
Amdt. dated November 19, 2004
Reply to Office action of September 22, 2004

Amendments to the Claims:

1. (Currently amended) A PN-junction varactor, comprising:
 - a first N-well formed on a semiconductor substrate;
 - 5 a first gate situated over said first N-well;
 - a first gate dielectric layer provided between said first gate and said first N-well;
 - a second gate situated at one side of said first gate and overlying said first N-well;
 - a second gate dielectric layer provided between said second gate and said first N-well;
 - a P⁺ doping region located in said first N-well between said first gate and said second
 - 10 gate, and serving as an anode of said PN-junction varactor, wherein said P⁺ doping region is encompassed by a second N-well, and wherein said second N-well has a doping concentration that is higher than that of said first N-well;
 - a first N⁺ doping region located at one side of said first gate that is opposite to said P⁺ doping region within said first N-well; and
 - 15 a second N⁺ doping region located at one side of said second gate that is opposite to said P⁺ doping region within said first N-well, and said second N⁺ doping region being electrically coupled to said first N⁺ doping region for serving as a cathode of said PN-junction varactor.
- 20 2. (Canceled)
3. (Original) The PN-junction varactor according to claim 1 further comprising a first N type lightly doped drain (NLDD) region merged with said first N⁺ doing region and wherein said first NLDD region extends to said first gate.
- 25 4. (Original) The PN-junction varactor according to claim 1 further comprising a second NLDD region merged with said second N⁺ doing region and wherein said second NLDD region extends to said second gate.

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5. (Original) The PN-junction varactor according to claim 1 wherein spacers are provided on sidewalls of said first gate and second gate.

5 6. (Original) The PN-junction varactor according to claim 1 wherein a salicide layer is formed on said first gate, said second gate, said first N⁺ doing region, said second N⁺ doing region, and said P⁺ doping region.

7. (Original) The PN-junction varactor according to claim 1 wherein, in operation, said
10 first gate and said second gate are grounded.

8. (Currently amended) A PN-junction varactor, comprising:

a first ion well of first conductivity type formed on a semiconductor substrate of second conductivity type;

15 a first dummy gate formed over said first ion well;

a first gate dielectric layer between said first dummy gate and said first ion well;

a second dummy gate formed over said first ion well at one side of said first dummy gate;

20 a second gate dielectric layer between said second dummy gate and said first ion well;

a first heavily doped region of said second conductivity type located in said first ion well between said first dummy gate and said second dummy gate, said first heavily doped region of said second conductivity type serving as an anode of said PN-junction varactor, wherein said first heavily doped region is encompassed by a second ion well of said first conductivity type, and wherein said second ion well has a doping concentration that is
25 higher than that of said first ion well; and

second heavily doped regions of said first conductivity type located in said first ion well at one side of said first dummy gate that is opposite to said first heavily doped region and at one side of said second dummy gate that is opposite to said first heavily doped

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region, said second heavily doped regions being electrically connected to each other and serving as a cathode of said PN junction varactor.

5 9. (Original) The PN-junction varactor according to claim 8 wherein said first conductivity type is N type, and said second conductivity type is P type.

10. (Original) The PN-junction varactor according to claim 8 wherein, in operation, said first dummy gate and said second dummy gate are grounded.

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11. (Canceled)

12. (Original) The PN-junction varactor according to claim 8 further comprising a lightly doped drain (LDD) formed in said first ion well, and wherein said LDD is merged with
15 said second heavily doped regions and laterally extends to said first/second dummy gates.

13. (Original) The PN-junction varactor according to claim 8 wherein spacers are provided on sidewalls of said first dummy gate and second dummy gate.

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